A Silicon BiCMOS Transceiver Front-End MMIC Covering 900 and 1900 MHz Applications*

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ABSTRACT

A Silicon BiCMOS transceiver front-end consisting of a low noise amplifier, power amplifier, and SPDT switch is described. The chip runs off a 5 V supply and requires a single CMOS/TTL control line for switch control. The LNA path has a 22 dB gain and 4 dB noise figure at 900 MHz. The PA has a gain of 22 dB and a output power of 15 dBm. The SPDT switch has an insertion loss of 1.3 dB, and an isolation of 22 dB at 900 MHz.

INTRODUCTION

Motivated by the expanding markets at higher frequencies, the Silicon industry continues to scale down device geometries and thereby scale up operating frequencies. Thus, advanced Silicon devices can now operate at frequencies which in the past were relegated to GaAs devices. For commercial applications, MMIC cost is an important driver which favors the lower cost Silicon technologies.

This paper describes a transceiver front-end MMIC implemented in an advanced BiCMOS process. The process includes NPN devices with an Ft of 12 GHz, and NMOS/PMOS devices with L_{eff}=0.45 um. The MMIC includes an LNA, PA, and SPDT switch operating from 600 to 2000 MHz and, thus, covering important commercial frequency bands. The chip is 2.1x0.9mm in size.

PASSIVE COMPONENT CONSIDERATIONS

In addition to the active devices the process also includes, inductors which can be implemented with up to 5 metal levels, MOS capacitors, MIM capacitors, and Polysilicon resistors. This BiCMOS process includes a buried P+ layer which has the effect of bringing the ground plane to within microns of the active devices and passive components on the chip surface. While this layer is beneficial for the bias isolation of NMOS devices, it increases the parasitic capacitances to ground associated with devices and components. To increase the useful operating frequencies of the passive components, the P+ buried layer was "masked out" of surface areas that include MIM capacitors, and inductors.

FRONT-END MMIC DESIGN AND MEASUREMENT RESULTS

A block diagram of the front-end is shown in Figure 1. The chip includes an LNA,

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PA, and SPDT switch. Figure 2 shows a photograph of the completed chip which is 2.1x0.9 mm in size.

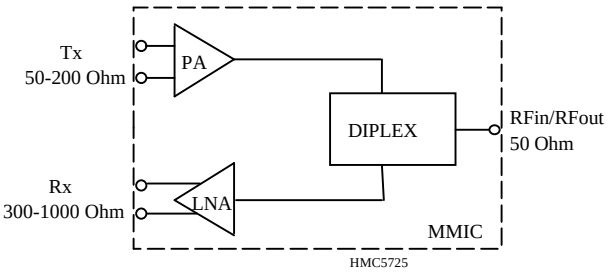

Figure 1. Front-End block diagram.

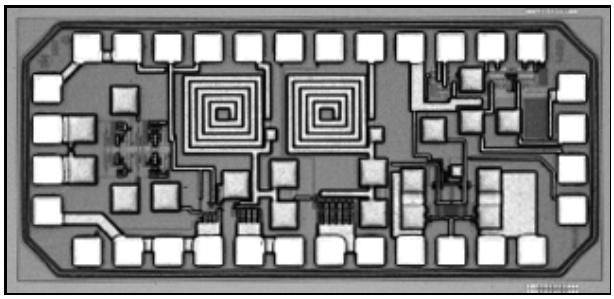

Figure 2. This chip photo shows the Silicon Front-End MMIC it measures 2.1x0.9 mm in size.

LNA DESIGN AND MEASUREMENT

The LNA is designed to have a single ended input and differential output to drive a balanced mixer. It consists of a common emitter NPN first stage, and a single ended to differential bipolar output stage. Device periphery and bias conditions were optimized for low noise figure. A series feedback inductor was also used to transform the input impedance closer to the noise match. The second stage was designed to provide a differential output impedance of 600 Ohm. The gain and noise figure of the LNA to antenna (ANT) path are shown in Figure 3. The current consumption of the LNA is 32 mA. The gain slopes from 22 dB to 15 dB in the frequency range from 0.6-2 GHz. This is a result of the use of resistive loads in both stages of the LNA.

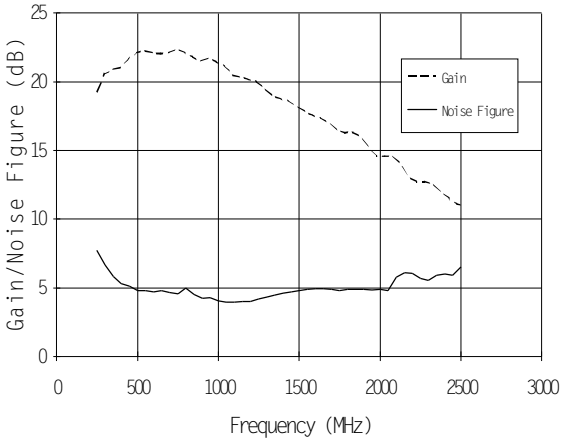

Figure 3. The path from antenna to the output of the LNA has a gain greater than 10 dB from 500 to 2000 MHz. The noise figure is less than 5 dB over this range.

PA DESIGN AND MEASUREMENT

The PA is designed to have differential input and single ended output. The first two stages consist of tapered differential NMOS stages with resistive loads and emitter follower buffers. The third stage consists of a single ended common source stage with a resistive load and emitter follower buffer. Finally, the last two stages consist of common source NMOS stages with tuned LC loads. Figure 4 presents the gain versus frequency for the two switch states. Note the gain exceeds 20 dB from 1 to 2 GHz, in the ON state of the switch. In the OFF state the isolation is better than 20 dB. The current consumption of the PA is 142 mA. The output power at the 1 dB compression point is 14 dBm as presented in Figure 5.

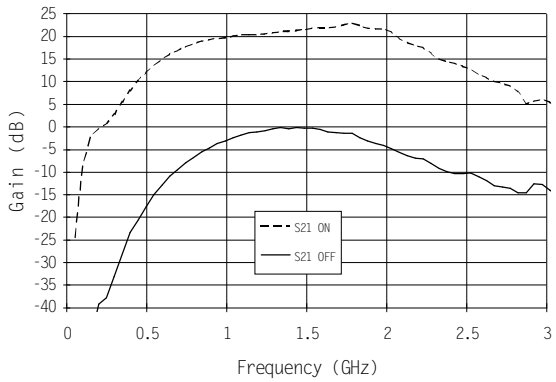

Figure 4. The gain from the PA input to the antenna output is greater than 15 dB from 600 to 2400 MHz. When the SPDT switch is toggled the switch provides 20 dB of isolation.

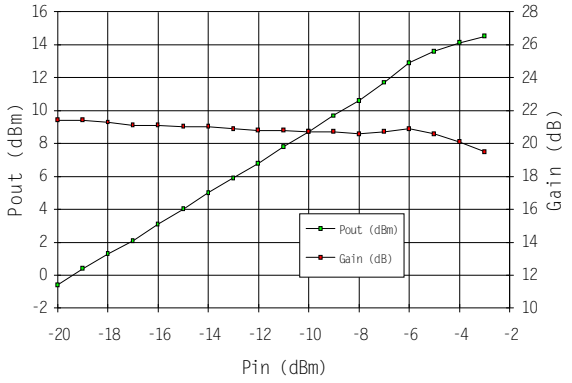

Figure 5. The power performance of the PA path is shown in this figure. The 1 dB compression point is 14 dBm. This measurement was done at 1.7 GHz.

SPDT SWITCH DESIGN AND MEASUREMENT

The SPDT design uses NMOS devices in a series shunt configuration. The shunt arm consists of an NMOS device in series with a 45 Ohm resistor to provide a match to the "OFF" throw arm. The channel is biased at 2.5 Volts to enable the switch to pass 18 dBm without distortion. Therefore, DC blocking capacitors are required on the switch ports. A chip consisting of the switch alone was constructed and measures 0.6x0.75 mm. The chip includes ground path blocking capacitors and a single ended CMOS driver. Figures 6, 7, and 8 show the measured insertion loss, isolation, and return loss of the chip. At 1 GHz the insertion loss is 1.3 dB, and the isolation is 29 dB. The 1 dB compression point of the switch is 22 dBm at 500 MHz as seen in Figure 9.

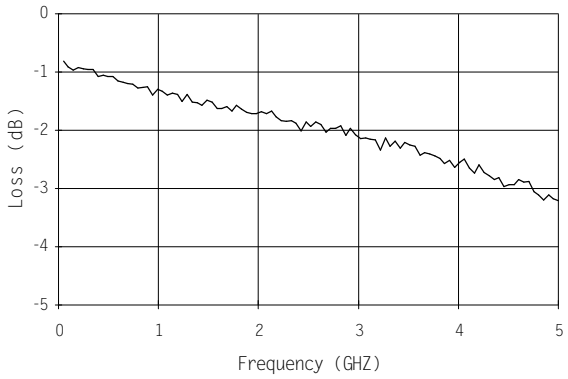

Figure 6. A test cell of the switch alone was measured. The insertion loss of the switch is 1.3 dB at 1 GHz.

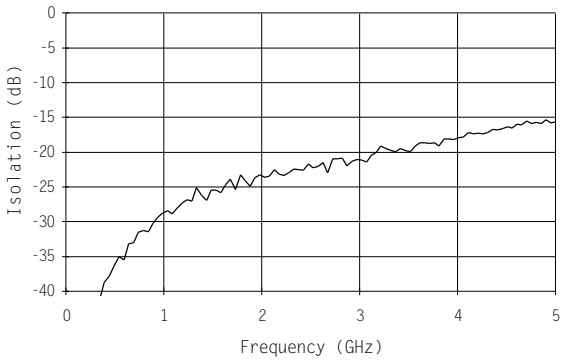

Figure 7. A test cell of the switch was measured. The isolation of the switch is 29 dB at 1 GHz.

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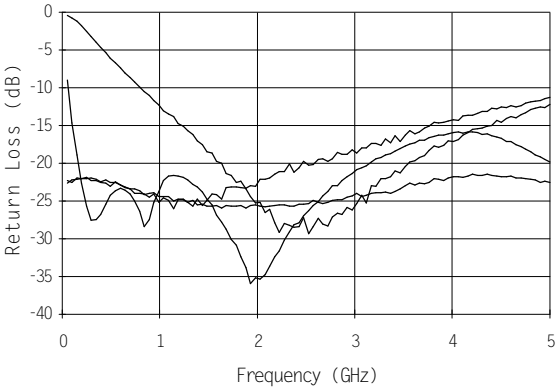

Figure 8. A test cell of the switch alone was measured. The port return losses are shown above. The return loss is better than 10 dB from 0.7 to 5 Ghz.

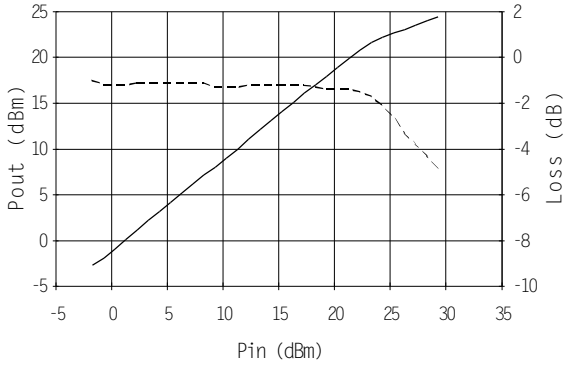

Figure 9. A test cell of the switch alone was measured. The switch has a 1dB compression point of 22 dBm at 500 MHz.

CONCLUSIONS

This work demonstrates the feasibility of using BiCMOS Silicon technology for the implementation of MMIC components for commercial applications at 900 and 1900 MHz. The BiCMOS process provides the possibility of integrating ECL and/or CMOS logic, as well as, analog front-end functions on a single MMIC.

ACKNOWLEDGEMENTS

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